Total No. of Questions : 12]

SEAT No :

P2801

[Total No. of Pages :3

[5154]-183
B.E. (Computer)
ADVANCED COMPUTER ARCHITECTURE
(2008 Course) (Semester-II) (410449)

Time : 3 Hours *Max. Marks : 100*

Instructions to candidates:

1) ***Answer any three questions form each section.***
2) ***Answer to these sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right side indicate full marks.***
5) ***Assume suitable data if necessary.***

SECTION-I

Q1) a) What are different classification approaches for parallel computer Architectures? Describe sample architectures representing each classification approach. **[10]**

b) How Branch prediction and speculative loading improves performance speedup of Itanium processor? **[08]**

OR

Q2) a) Define Amdahls law. Derive an expression for CPU clock as a function of instruction count, clocks per instruction and clock cycle time. **[10]**

b) Explain the following terminologies associated with SIMD computers. **[8]**

i) Lock -step Operations.
ii) Associative Memory.
iii) Adjacency search.
iv) Bit serial Assocative processor.

Q3) a) With suitable example, describe the major hurdles of pipelining. **[8]**

b) Find the set of distances and the collision vector for the reservation table shown below. **[8]**

	0	1	2	3	4	5	6	7
S1	1			1		1		
S2		1	1		1			
S3				1				1

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OR

Q4) a) What is significance of dynamic prediction? Draw the state transition diagrame for 2 bit prediction scheme. **[8]**

b) How to overcome the data hazards with dynamic scheduling? **[8]**

Q5) a) Discuss with example any three vectorizing functions designed for optimizing compilers. **[8]**

b) How array processing is different than vector processing?Discuss the basic architecture of ILLIAC-IV Model 1 array processor. **[8]**

OR

Q6)a) State the concept of pipeline chaining. What is vector looping? With example explain vector looping with respect to Cray-1architecture. **[8]**

b) What is the use of data routing functions? With example discuss the necessity of data routing in array processors. **[8]**

SECTION-II

Q7) a) With a neat diagram, explain the basic structure of a centralized shared memory and distributed memory multiprocessor. **[10]**

b) Explain snooping with respect to a cache coherence protocols. **[8]**

OR

Q8) a) Explain the symmetric shared memory architecture, in detail. **[10]**

b) Describe distributed shared memory and directory based cache coherence. **[8]**

Q9) a) What are multi-threaded architectures? Discuss the various performance parameters of multi-threaded processor architectures. **[8]**

b) State the following terms w.r.t. multithreaded architectures:

i) Interleaved Multithreading

ii) Latency Hiding

iii) Context Switching

iv) Efficiency. **[8]**

OR

Q10)a) What is latency hiding? Explain any Two methods used for Latency Hiding in multi-threaded architectures. **[8]**

b) With example explain message passing parallel programming.What is SPMD programming? **[8]**

Q11) Discuss the requirement of language features for parallel programming. Describe the various issues to be handled in parallelizing compiler with respect to flow analysis, optimization and code generation. **[16]**

OR

Q12) a) Explain in detail the steps usually followed for generating a multiprocessing application from a sequential application. **[8]**

b) Explain the fork and join mechanism in any of the parallal languages. Where is this method most useful. **[8]**

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